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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,448	11/19/2003	Hideyuki Matsuoka	XA-9989	3935

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/715,448	MATSUOKA ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1103*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 11/19/2003 through 12/29/2004, claims 120 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 11/19/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Foreign Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

4. The drawings are objected to for the following reasons.

Figures 2-7 are not designated by a legend such as "Prior Art". The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation: "a memory cell including a transistor disposed between the first word line and the bit line and a magnetic resistance element disposed between the second word line and the bit line" (claims 1-2) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5. A proposed drawing correction or corrected drawings, showing changes in red ink, are required in reply to the Office Action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. However, formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner (see MPEP § 608.02v).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-2 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 2 comprises limitation: "a memory cell including a transistor disposed between the first word line and the bit line and a magnetic resistance element disposed between the second word line and the bit line". Neither the specification nor the drawings describes such limitation.

Claims 1-2 contain the limitation "the magnetic resistance element is formed into a pillar-like shape by patterning a plurality of layered structures formed on the semiconductor substrate". Nowhere in the specification describes such limitation.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim(s) 13-17 is/are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, lines 15-16, the limitation "the word line being a gate electrode of the vertical type transistor" regards only one word line, wherein a plurality of word lines are

previously claimed. Thus it is not clear of which word line is the gate electrode of the vertical type transistor?

Claim 15 and 19 recite the limitation "the second word line". There is insufficient antecedent basis for this limitation in the claims.

Claims 14-17 depend from rejected claim 13 and include all of the limitations of claim 13 thereby rendering these dependent claims indefinite.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claim(s) 1-20 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,560,135 to Matsuoka et al.

Regarding claim 1, Matsuoka discloses a magnetic semiconductor memory device, as shown in figs. 7-45, comprising:

a semiconductor substrate 1707;

first and second word lines 805 and (705 or 1304) arranged in parallel to each other on the semiconductor substrate 1707;

a bit line 605 crossing the first and second word lines via an insulator layer; and

a memory cell including a transistor (comprising layers 1006/1901/1007) disposed between the first word line 805 and the bit line 605 and a magnetic resistance element (formed by layers 25/26/27) disposed between the second word line and the bit line;

wherein the magnetic resistance element (25/26/27) is formed into a pillar-like shape by patterning a plurality of layered structures formed on the semiconductor substrate, and at

least the side surface is covered with the second word line via the insulator layer. See figs. 30-45 and col. 8, line 49 to col. 10, line 13.

Regarding claim 2, Matsuoka discloses a magnetic semiconductor memory device, as shown in figs. 7-45, comprising:

a semiconductor substrate 1707;

first and second word lines 805 and (705 or 1304) arranged in parallel to each other on the semiconductor substrate 1707;

a bit line 605 crossing the first and second word lines via an insulator layer; and

a memory cell including a transistor (comprising layers 1006/1901/1007) disposed between the first word line 805 and the bit line 605 and a magnetic resistance element (formed by layers 25/26/27) disposed between the second word line and the bit line;

wherein the magnetic resistance element (25/26/27) is formed into a pillar-like shape by patterning a plurality of layered structures formed on the semiconductor

substrate 1707, and the top surface and two side surfaces are covered with the second word line via the insulator layer. See figs. 30-45 and col. 8, line 49 to col. 10, line 13.

Regarding claims 3 and 18, Matsuoka discloses a magnetic semiconductor memory device wherein the direction of an electron traveling in a channel area is perpendicular to the main surface of the semiconductor substrate in the transistor. See fig. 24-27.

Regarding claim 4, Matsuoka discloses a magnetic semiconductor memory device wherein a channel is made of polycrystalline silicon in the transistor. See col. 9, lines 5-22.

Regarding claims 5 and 14, Matsuoka discloses a magnetic semiconductor memory device wherein at least the upper surface of the bit line is covered with a soft magnetic film. See fig. 45 and col. 10, lines 5-13.

Regarding claims 6, 15, and 20, Matsuoka discloses a magnetic semiconductor memory device wherein at least one surface of the second word line is covered with a soft magnetic film. See fig. 45 and col. 10, lines 5-13.

Regarding claim 7, Matsuoka discloses a magnetic semiconductor memory device, wherein the magnetic resistance element is a layered structure including a

ferromagnetic material, a tunnel insulator film and a ferromagnetic film. See col. 9, line 60 to col. 10, line 4.

Regarding claims 8 and 19, Matsuoka discloses a magnetic semiconductor memory device wherein the second word line surrounds the bit line in at least three directions via the insulator film. See figs. 29.

Regarding claim 9, Matsuoka discloses a magnetic semiconductor memory device wherein the soft magnetic film is permalloy ($Ni_{81}Fe_{19}$).

Regarding claim 10, Matsuoka discloses a magnetic semiconductor memory device wherein the bit line extends between the first and second word lines. See figs. 30-45.

Regarding claim 11, Matsuoka discloses a magnetic semiconductor memory device wherein the bit line extends between the second word line and the magnetic resistance element. See figs. 30-45.

Regarding claims 12 and 16, Matsuoka discloses a magnetic semiconductor memory device wherein the magnetic resistance element is formed into a rectangular shape having short sides and long sides, the direction of the long side being perpendicular to the bit line. See figs. 30-45.

Regarding claim 13, Matsuoka discloses a magnetic semiconductor memory device, as shown in figs. 20-29, comprising:

a semiconductor substrate 1704;

a plurality of word lines 804 formed on the semiconductor substrate 1704;

a plurality of bit lines 604 crossing the plurality of word lines 804; and

a memory array including memory cells arranged at crossing points between the plurality of word lines 804 and the plurality of bit lines 604;

wherein the memory cell includes a vertical type transistor (formed by layers 1004/19/1005) having a channel area 19 formed in a direction perpendicular to the main surface of the semiconductor substrate 1704 and a magnetic resistance element 505 disposed above the vertical type transistor, the word line 804 being a gate electrode of the vertical type transistor and covering at least two side surfaces of the magnetic resistance element 505 via an insulator film. See also col. 7, line 14 to col. 8, line 47.

Regarding claim 17, Matsuoka discloses a magnetic semiconductor memory device wherein a spin flips its direction by varying the direction of a current flowing in the bit line, thus reversing data accordingly. See col. 1, line 13 to col. 2, line 57.

Conclusion

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
April 15, 2005